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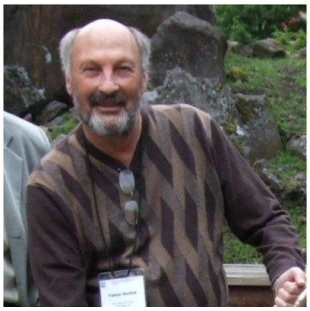

Доктор **Ихель Готкис** является признанным высококомпетентным химиком, физиком и технологом мирового уровня в области полупроводников с богатым опытом в современных областях полупроводниковой промышленности, включая производственный опыт работы на Интель FAB8. Его образование включает химию, физику, материаловедение, химическую и полупроводниковую технологии.

И. Готкис получил степень магистра в 1970 г и степень кандидата наук по физической химии в 1975 г. Обе степени получены в ИГХТУ. С 1970 по 1989 г работал в ИГХТУ в группе проф. К.С. Краснова. В 1981-1984 гг. работал на кафедре физической химии Еврейского университета Иерусалима (Израиль). И в 1994 г начал свою карьеру в промышленности в корпорации Интель. В 1977 г поступил на работу в американскую компанию IPEC (позднее Novellus Corp. и затем Lam Research Corp.), переехал в США и начал работать в компаниях главных поставщиков оборудования производства микросхем (Lam Research Corp. и KLA-Tencor Corp., Силиконовая Долина, Калифорния) в отделе исследований и разработок производства полупроводников.

Доктор И. Готкис получил более 140 патентов и опубликовал более 50 статей в ведущих научных и промышленных журналах. Он являлся приглашенным лектором ряда главных профессиональных форумов. Является обладателем престижной государственной премии Израиля за научные достижения (1993 г.), которая была вручена ему Президентом Израиля Хаимом Герцогом.

НЕКОТОРЫЕ АСПЕКТЫ ПРОИЗВОДСТВА ПОЛУПРОВОДНИКОВЫХ МИКРОСХЕМ: ЗАКОНЫ МУРА, МЕЖДУНАРОДНАЯ ТЕХНОЛОГИЧЕСКАЯ КАРТА ДЛЯ ПОЛУПРОВОДНИКОВ И ОСНОВНЫЕ ВЫЗОВЫ В СОВРЕМЕННОЙ ТЕХНОЛОГИИ ПРОИЗВОДСТВА ИНТЕГРАЛЬНЫХ МИКРОСХЕМ

В данном кратком обзоре рассматриваются и обсуждаются некоторые главные проблемы производства полупроводниковых микросхем, такие как 1-й и 2-й законы Мура, международная технологическая карта для полупроводников, последние тренды технологии производства, исследования и развитие и текущие производственные вызовы такие как проблемы фундаментальные (Пуассоновский дробовой шум – статистическая флюктуация- для ряда частиц типа атомов, заполняющих элементарный безразмерный объем), технологические проблемы –улучшенная технология структуры и литография экстремального ультрафиолета, конструирование оборудования для производства современных микросхем и имеющие к этому отношение бизнес факторы (экстремально высокая стоимость производства и возможности исследований и развития).

Ключевые слова: полупроводники, микросхема, SoC, законы Мура, международная технологическая карта для полупроводников, технология производства микросхем, исследование и развитие полупроводников, полупроводниковый бизнес

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Dr. **Yehiel Gotkis** is a recognized highly competent chemist, physicist and world class semiconductor technologist with extended experience in advanced sectors of semiconductor industry including production line at Intel FAB8. His background is in Chemistry, Physics, Material science, SC technology and Chemical Engineering.

Y. Gotkis earned his M.Sc. (ХТВМиП) in 1970 and PhD in Physical Chemistry in 1975, both from ISUCT (ИХТИ, that time). He worked at ISUCT in the group of Prof K.S. Krasnov from 1970 to 1989, when he moved to Israel. In Israel he worked for Hebrew University of Jerusalem (1981-1984, Dept. of Physical Chemistry) and in 1994 started his career in industry at Intel Corp. In 1997 he was hired by an US company (IPEC, which became later Novellus Corp. and then Lam Research Corp.) and moved to US where he worked for the major chip fabrication equipment providers (Lam Research Corp. and KLA-Tencor Corp., both in Silicon Valley, California), leading SC process R&D.

Dr. Y. Gotkis has numerous (140+) granted patents, and publications (50+) in major academic and industrial journals and invited talks and presentations at major professional forums. Among his achievements is a prestigious State of Israel Award for Scientific Achievements (1993) presented to him by Haim Hertzog, that time President of State of Israel.

SOME QUICK NOTES ABOUT SEMICONDUCTOR CHIPS FABRICATION: MOOR'S LAWS, INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS) AND MAJOR CHALLENGES IN THE STATE-OF-THE ART INTEGRATED CIRCUIT (IC) FABRICATION

Some general aspects of the semiconductor chips fabrication, such as Moor's law-1 and Moor's law-2, ITRS roadmap, latest trends in the advanced product and fabrication technology R&D, and industry current challenges, like problems of fundamental scientific nature (structural: Poisson shot noise (statistical fluctuation) in the number of species, like atoms, filling a smallest elementary node-sized cube), of technological nature (advanced patterning technology and Extreme Ultra-Violet, EUV, Lithography), of advanced chip fabrication equipment engineering and of associated business factors (extremely high costs of production and R&D facilities) are presented and discussed in this quick review.

Key words: semiconductors, micro-chip, SoC, Moor's laws, ITRS, micro-chip technology, semiconductor R&D, semiconductor business

INTRODUCTION

The purpose of these quick notes is to share with the readers my views on some hot matters related to the current state of the semiconductor (SC) industry for which I worked for about 20 years.

The SC chip fabrication companies live by a "simple doctrine: smaller, faster, cheaper, over…" [1]. The benefit of this tetrad is straightforward: producing chips with more tightly packed tinier and faster primary functional features (transistors, capacitors, connectors etc.) means getting higher number of them onto a chip, and, as a result, higher number of advanced functionalities the chip is capable to support.

Due to fierce competition in the SC chip business space and new technologies, appearing "like mushrooms after a rain", and dropping R&D and production costs for a given chip generation, the price of a new "hot" chip can fall within a matter of months by 50% or so. As a result, there is a permanent pressure on chip makers to come up with something better than the just a few months old state-of-the-art. Even in a downturn cycle there is no excuse for them not to come up with better products to fulfil the customers'

appetite keen of boosting the capabilities of their computing and electronic devices. Traditionally, the key SC companies (Intel, Samsung, Toshiba, NEC…) preferring "to keep their cards close to the chest" tightly control their entire production process from design to manufacture. Yet, foundry companies, like TSMC, UMC, Global Foundries, whose sole business is manufacturing for customers, have come to the fore recent decades providing great outsourcing options for fabless companies and small start-ups. In addition to the giants, a large number of smaller specialized designing and chip fabricating and testing companies also appeared in the marketplace.

As far as the SC product spectrum is concerned, broadly speaking, it is made up of four main categories:

Memory chips serving as data storages to temporarily retain and/or to pass information to and from computer logic devices. The consolidation of the memory producers drove memory prices so low that only a few giants like Samsung, Toshiba, Micron, NEC can afford to stay in the game.

Microprocessors are central processing structures that support the basic logic functionalities performing the tasks. Intel's domination in this segment has forced nearly every other competitor, except AMD, out of the mainstream market into smaller niches or into different segments altogether.

Commodity ICs, sometimes called "standard chips", are produced in huge batches for routine processing purposes. Dominated by large Asian chip manufacturers, this segment offers tiny profit margins, so that only the biggest companies can survive in the competition.

Complex Systems on a Chip (SOC) are essentially IC chips with an entire system's capability on it. With the doors to the above mentioned (memory, microprocessor and commodity IC) markets segments tightly shut, the SOC segment at this point is the only one still left with opportunities for a wide range of companies.

MOOR'S LAWS AND THE ITRS

In 1971 Intel, that time not a well-known small company, released its first ever microprocessor, the 4004. The chip, sized 12 mm^2, contained 2300 transistors spaced by 10 μm gaps. To compare, the latest Intel IC product, the 10-core Intel® Core™ i7 64-bit Extreme Edition processor, being only about x10 larger than the 4004, provides unthinkable computing power [1-3], having several billion transistors at spacing of just 10-14 nm. Microchips, as components of consumer and industrial electronics, are used today everywhere from supporting conventional technologies to foreign policy, from booking hotels and flights to designing rockets and H-bombs. And certainly, the advanced microchips themselves and their fabrication technology…

The idea of a technology roadmap (RM) for semiconductors (SC) can be traced back to the paper by Gordon E. Moore, in which he, back in 1965, projected that the number of components that could be incorporated per IC would increase exponentially over time [3]. Since 1971, the number of functional components (transistors, capacitors etc.) per chip indeed has exponentially increased (doubled practically every two years), and this historical trend was widely accepted by the chip fabrication community, as a Moor Law (ML) [4].

The doubling period is frequently quoted as 18 months because of Intel executive David House, who predicted the overall chip performance (a combo effect of more transistors and their increased signal processing speed). Since that time the clock frequency increased roughly by 6 orders of magnitude from 10^5 Hz to 10^{12} Hz, doubling every 18 months [4].

Digital electronics has strongly contributed to world economic growth [4]. ML greatly stimulated and would still continue assisting chip fabrication industry in reduction of the manufacturing costs, while enabling the creation and production of more advanced devices. The macro-economic potential of ML has been displaying its power upon the world's economy by creating new jobs and inducing deflation. This long-term deflationary effect (when the price per a device function is declining, it is considered a deflationary effect) of SCs has never been fully accounted for in statistics and economics. As a deflation example, the reduction in computer cost and chip price per bit has been stunningly spectacular. In mid of 1950-s before the IC was introduced, the average selling price of a transistor was about $5,5. Fifty years later, the cost per bit of a Dynamic Random Access Memory (DRAM) chip dropped to an astounding one nanodollar. As the number of functional components (transistors, capacitors etc.) per chip increased, the total chip size was kept within practical and affordable limits agreed by the SC community to be not larger than 145 mm^2 for DRAMs and 310 mm^2 for microprocessor units (MPUs). As of 2016, the largest transistor count in a commercially available single-chip processor is over 7,2 billion - the Intel Broadwell-EP Xeon [5]. In other types of ICs, such as field-programmable gate arrays (FPGAs), the Altera Stratix 10 has the largest transistor count, containing over 30 billion transistors [4].

ML is widely considered to be a summarization of an observation or projection and not an actual physical or natural law.∗ It seems to be reasonably constant, given the point that companies normally invest a planned reproducible percentage of the revenues in the future product R&D. Especially the well-organized giants like Intel, Samsung, Toshiba etc. Or most probably the prestige to be following for any acceptable price the ML was forcing them to invest as high percentage of their profits as possible into the new advance products. Which for the well-planning their finances giants became a Year-over-Year (YoY) reasonably permanent maximum possible percentage (something close to semi-intuitive 20-25% of the profits). Thereby it sounds reasonably natural that since the early 70's, the Western SC industry ambition, prestige and ability to follow the ML trend acted as the engine and the catalyst of a virtuous cycle: through scaling one gets a better performance/cost of a product inducing some growth of the SC market, which, in its turn, fuels company's maximum possible investments in the scaling, and, as a result, providing to the market the next generation advanced products, which fuels further scaling R&D and so on. The ITRS RM effort has assumed the viability and extendibility of ML and the continuation of its remarkable cycling. Conversely, the RM has helped to sustain this advancing trend by identifying the knowledge gaps to be closed to allow it to continue, helping the R&D efforts to focus on the most impeding technology challenges. In general, ML should be considered as a driving force of the World technological and social progress, productivity, and econo-mic growth [4].

Nowadays the SC industry is facing an increasing importance of a new challenge, branded as "More than Moore" (MtM) [6], when device added value is provided by incorporating advanced integrated complex functionalities that do not necessarily scale as per the smallest functional element, as in the ML. At this point the MtM ITRS has started with a Rev0 projection law similar to that of ML, however, it becomes clear that a new different concept is going to be needed to identify and guide the MtM RM efforts. And it is also likely to require involvement of wider SC community beyond the ITRS actual members.

In this paper, a quick overview of a handful of most significant complications and bottlenecks known for advanced SC technological space is presented.

As far as the challenging points the SC industry faces these days, a corresponding list could be endless. In these short notes I am going to focus just on a very few of them, those, which, to my opinion, are among the most stumbling and painful ones, and which for this reason are to be in the main focus of R&D groups dealing with advanced products and technologies. Some of these challenges are based on the fundamental origins of materials and the others on advanced manufacturing hardware capabilities and technological process snags.

Generally speaking, ML is about the increasingly higher density of functional elements (transistors, capacitors etc.) packed onto a single piece of silicon of a limited predefined size. Even more generally, though, it means that the current complications impeding the development of an advanced product are resolvable. As they were in the past and as they going to be in the future. Sooner or later… depending on the amount of material and intellectual resources the company, or the industry as a whole, is ready to reinvest into finding solutions and developing new value-added products. This idea is frequently formulated as Continuous Improvement Principle (CIP), which is based on a Japanese concept called Kaizen [7] - the philosophy of constantly seeking for ways to improve the operations. It involves identifying best businesses and practices and instilling a sense of employee ownership of the process. The CIP is based on confidence that any element of product evolution starting from defining the new goals and design ideas to pilot production and final product fabrication can be improved and that the people most closely associated with the operations are the bests to identify the existing shortcomings and the necessary improvement changes to be made. Consequently, it points at the employee as the key player of the CIP. Setting the CIP philosophy as an integrated part of the corporate culture may be a lengthy and in some cases even a painful process. But it is worth going for it. The employee sense of ownership is central to the CIP helping them to consider themselves as owners of the process and methods they use and take pride of the high quality of the work they provide. Especially helpful to implement the CIP is employee actual participation in the variety of the short and long term problem solving activities, inspiring their sense of personal control over their workspace.

To provide the reader with a sense of the advanced SC R&D lifestyle, I would like to bring up a term very popular in the R&D environment, which is a conversion of the term "leading edge of technology"

∗ Although, to my opinion, it appears to follow a simple first order rate exponential equation, and we just need to understand the nature of the rate constant, which looks to me to be associated with the relative portion of business gains available to be invested into the advanced product R&D.

to the "bleeding edge…" [8], and which well represents the tight and tough, although professionally very exciting and fruitful, atmosphere of the advanced R&D activities packed with numerous taskforces, workshops, problem solving groups, deadlines etc., etc.

As far as the challenges, I planned to discuss, I selected just a few of them listed below, each belonging to a specific sector of the SC industrial space. Some are based on the fundamental origins of materials used in chip design and others on hardware limited capabilities or on new process development problems to be resolved:

- Materials fundamentals based limit: statistical instability of the number of hypothetically indivisible (like atoms) species filling the smallest ENSEs.
- Advanced fabrication and process monitoring equipment current technical complications based: advanced patterning (lithography&plasma etch).
- SC business environment. Globalization matters. High production and R&D facilities costs. Cyclic nature of the SC business.

MATERIALS FUNDAMENTALS BASED LIMIT: THE NUMBER OF HYPOTHETICALLY INDIVISIBLE (LIKE ATOMS OR MOLECULES) SPECIES FILLING A SINGLE ENSE ELEMENT BECOMES STATISTICALLY UNSTABLE

Technologists now believe that new generations of advanced chips will be created ever slower, and by the middle of the next decade the SC technology could hit a hard wall, when the most basic laws of physics will not allow the chips of the current basic architecture, by then composed just by a handful of atoms, to function reliably. At this point ML will stop working. Unless a new conceptual breakthrough occurs…

It is Siméon Denis Poisson [9] "to blame" for this bottleneck (See the Fig. 1, a copy from [9], and explanations in the associated caption.

In the high yield manufacturing, as chip fabrication is, even common sense "low" probabilities could be still high enough to affect the yield.

Switching to Fig 2. let us assume that industry at the moment is running its High Volume Production (HVP) at 10 nm node and the most stringent material used in the product stack consists of atomic or molecular spheres of 0.5 nm in diameter, like, for example, metal oxides or nitrides, and let us calculate the Poisson fluctuations for the number of atoms within the ENSE volume for the current 10 nm node and the future 7 nm, 5 nm and 3 nm nodes. The assumed atomic size allows to package for each node in average of 8000, 3400, 1000 and 200 atoms per corresponding ENSE volume. Also, let us assume, that it was found during the 10 nm node technology R&D that the yield loss starts to show up when the ENSE is filled with the assumed spheres by less than 75% of its volume.

The Poisson 25% shortage probabilities for a single ENSE element (colored curves and data points) and related numeric data for the four mentioned nodes together with probabilities for a 10 km integrated length interconnect network of the node-sized lines are shown below the graph. The trend illustrates that the probability of yield loss, being extremely low and not affecting the yield for the 10 nm node lines, quickly increases potentially becoming a complete yield killer for the 3 nm node. And even for the 5 nm node, the yield loss probability, keeping in mind that the 25% shortage assumption was in a way made out of blue, should be considered as marginally low. Indeed, if it was 20%, instead of 25%, then the yield loss probability for the 5 nm node would also jump into the yield kill zone. So, these estimations, even being quite rough, show that the 3 nm and probably the 5 nm nodes seem to be under danger of not meeting the HVM yield specifications due to the Poisson shot noise. Thereby, motivated by the CIP, the R&D teams, moving forward and not foreseeing a more suitable material with a substantially smaller atomic size to replace the assumed one, should consider exploring alternative, but ML shrinkage, venues.

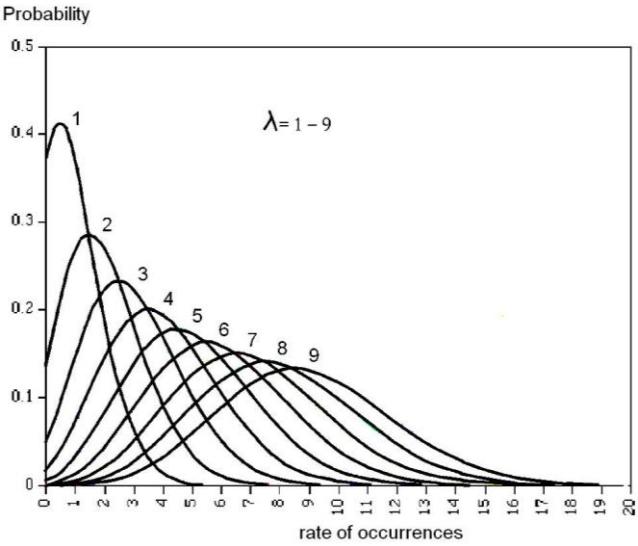
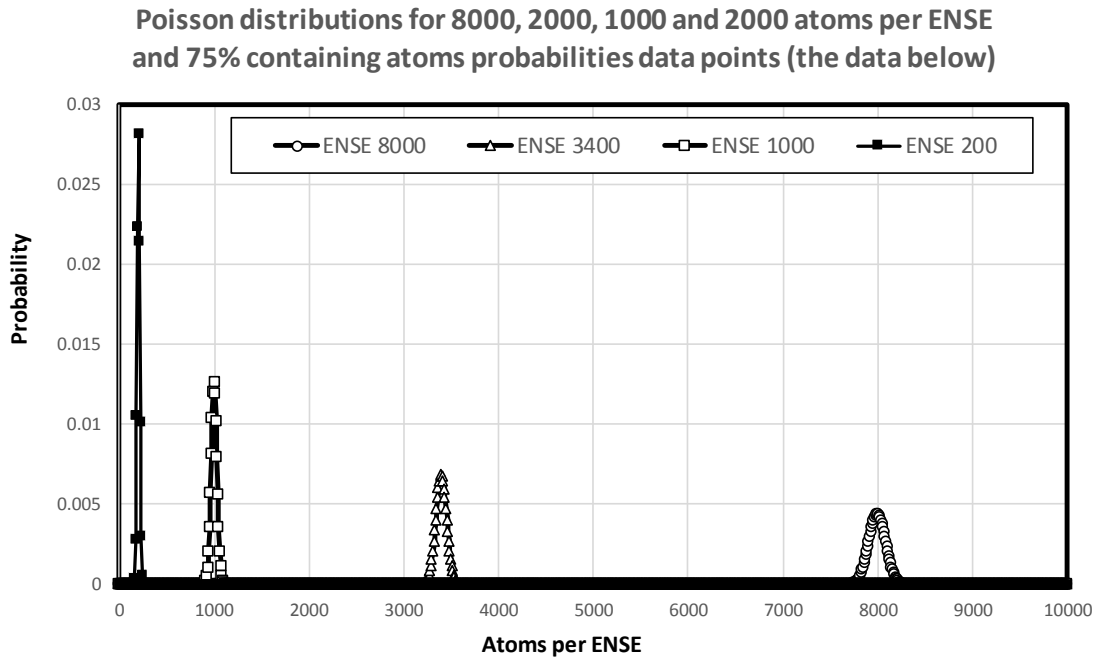


Fig. 1. Poisson distributions for several rate of occurrences of some event, λ, from 1 to 9. In the cases where the λ is small, the range of probabilities will approach and intercept the zero occurrence border (vertical axes) at some "observable" value. As the λ becomes higher, eventually, somewhere around λ = 7, zero occurrences get to some very low (but yet not absolutely zeroed) probabilities

Рис. 1 Распределения Пуассона для нескольких частот/вероятностей реализации некоторого (наблюдаемого) события, λ, от 1 до 9. При малых λ интервал вероятностей приближается к оси "нулевой реализации" и пересекает её при некотором конкретном значении вероятности. При больших λ (около 7) нулевые реализации становятся всё менее вероятными, но всё же не абсолютно нулевыми



	Atoms per ENSE	8000	3400	1000	200
	20% at. Loss	6000	2550	750	150
	Prob. of a corrupted ENSE	5.69E-122	2.19E-53	1.97E-17	3.46E-05
	Prob. of a corrupted chip	5.69E-110	3.07E-41	3.93E-05	**1.14E+08**

Fig. 2. Poisson distributions and ENSE and chip loss probabilities for assumed 10 nm (8000 at/ENSE), 7 nm (3400 at/ENSE), 5 nm (1000 at/ENSE), and 3 nm (200 at/ENSE) nodes, and relevant 75% atomic content probability values as defined in the picture
Рис. 2. Распределения Пуассона для рассмотренного в тексте числа атомов в Элементаром Квадратном Размерном Элементе (ENSE , см. аббревиатуру в тексте) и вероятности потерь чипов для предположенных 10 nm (8000 at/ENSE), 7 nm (3400 at/ENSE), 5 nm (1000 at/ENSE), и 3 nm (200 at/ENSE) технологий, и соответствующие вероятности 75% (атомного) ENSE заполнения

One may say that one day some advanced architectures could be developed allowing to stay away of that small ENSEs. Which is almost right. Almost, because there are some structural features, which, within the node definition, cannot be changed. These are the interconnect [10] wires and interlayer contacts. Their network, having quite an extended integrated length, roughly in the 10 km range, with equivalent number of ENSEs as high as 10^{12} elements, making the interconnect wires to be especially predisposed to be affected by the Poisson shot noise, potentially causing a variety of yield and reliability issues, like disconnects, increased RC delay, local heating, electro migration and so on.

ADVANCED FABRICATION AND PROCESS MONITORING EQUIPMENT COMPLEXITY BASED: ADVANCED PATTERNING (LITHOGRAPHY [11])

General. One of the most, if not the most, challenging operation in chip fabrication is patterning, which is performed by lithography and etch tandem, the lithography being the key critical step. In complex ICs, a wafer will go through the photolithographic cycle up to 50 times. In the modern advanced deep UV (DUV) lithography a special class of photoresists, so-called chemically amplified resists (CARs) [12], are normally used. Among other components, CAR resist composition contains so-called acid generator molecules, AGs, which, under the UV irradiation convert to carboxylic acids catalyzing resist polymer solubility in a basic developer.

As we spoke above, the ML has resulted in dramatic improvements in computing power over multiple decades. However, as 193 nm immersion optical lithography (IL) [13] has been running out of steam even being enhanced by multiple patterning (MP) [14], production costs have become the primary scaling obstacle. In its simplest approach the 193 nm DUV lithography started to see problems at nodes of 45 nm or so, and numerous technological advances, as MP and IL DUV processing helped to extend its applicability limit down to 14 nm node. However, at this point the high operational costs started to push technologists to look towards the Extreme UV (EUV) lithography [15].

The EUV lithography, which at some point began to be seen as panacea for key layers patterning, also has failed to be cost-effective for the 14 nm node, however, still leaving hope it may become a winning approach for the 7 nm one. The non-EUV layers assume conventional MP IL schemes, for example, 193nm IL based litho-etch-litho-etch (LELE) [16].

MP is expected anyway to be used even by EUV for random logic patterns at the 7 nm node, the 5 nm node [17] would almost certainly need to use MP, which is already developed and working with IL DUV.

The ability to project a clear image of a smallest feature onto the wafer, the resolution parameter, is limited by the wavelength λ of the light used and the numerical aperture *NA*, the ability of the lens system to capture enough diffraction orders from the illuminated mask. The current state-of-the-art photolithography tools use DUV light from excimer lasers with wavelengths of 248 nm or 193 nm, which allow patterning features down to 50 nm.

The minimum feature size that a projection system can print is given approximately by formula:

$$CD = k_1(\lambda/NA),$$

where *CD* is the minimum feature size (also called the critical dimension (*CD*), design node rule), k_1 (commonly called k_1 factor) is an integrated coefficient that encapsulates all process-related factors and normally equals 0,4 for HVM conditions, λ is the wavelength of the light, *NA* is the numerical aperture of the lens as seen from the wafer.

According to the above equation, minimum feature sizes can be decreased by decreasing the wavelength, and increasing the numerical aperture (to achieve a tighter focused beam and a smaller spot size). However, this method runs into a competing depth of focus, D_F, constraint:

$$D_F = k_2\ (\lambda/(NA)^2),$$

where k_2 is another process-related coefficient (k_2 *factor*).

The D_F depth of focus limits the thickness of the photoresist and the depth of topography on the wafer. Chemical Mechanical Planarization (CMP) [18] is normally used to planarize the surface topography prior to high-resolution lithographic steps.

The EUV, having the photon wavelength of λ = 13,5 nm, was and still is hopefully considered to be the next-generation lithography. It is currently being under intense development for possible future planned HVM use in 2020 by Intel's, Global Foundries' and Samsung's 7 nm node, TSMC's 5 nm node and SMIC's 14 nm node. However, there is a number of challenges still required to be resolved.

EUV light source. As of today, the established EUV light source is a Sn laser-pulsed plasma (LPP) [15], where the source of 13,5 nm light is a dynamic population of multiple-charged Sn^{+9} - Sn^{+13} ions, which, recombining with electrons, emit light of several wavelengths including 13,5 nm. The satellite photons have to be filtered out, which reduces the efficiency of "useful" light generation. LPP is generated by microscopic droplets of molten Sn shattered by powerful laser pulse. LPP sources outputs (e.g., ASML's NXE:3300B scanner) exceed 250 W - the minimum requirement for a reasonable throughput. However, for the HVM the EUV LPP sources need to be significantly overpowered, on the order of 10^{11} W/cm^2 indicating the enormous energy burden imposed. An EUV source driven by a 200 kW CO_2 laser consumes an electrical power of about 2 MW, while, in comparison, a conventional 100 W ArF IL laser consumes 20 times less energy, only about 10 kW.

Another complication of the EUV sources is related to the mentioned above photons incoherency [15]. The necessity to convert the as it is incoherent light to as much monochromatic as possible is associated with satellite photons filtering and additional associated energy losses.

Nevertheless, after many years of uncertainty regarding the suitability of the EUV source for HVM lithography, it finally started to show some signs of getting closer to the HVM readiness. Recent increases in the power and availability of LPP sources almost eliminated the uncertainty concerning the laser power and many of the recent studies turned to search for the EUV insertion solutions (node and process layers) and extendibility.

An alternative free-electron laser (FEL) EUV source concept, introduced some time ago, promising to be cost effective single-source alternative for powering a manufacturing FAB's entire EUV lithography module, is under intense development, as well.

Optics and mask. As it was highlighted above, the source power still is the dominating concern for HVM, however, significant improvements in EUV optics and mask fabrication and supporting infrastructure, including blanks, pellicles and inspection tools, also require close attention and are also under intense R&D at this point.

Any matter absorbs EUV radiation. Hence, EUV lithography working conditions require high vacuum. All optical elements, including the photomask, must use defect-free Mo/Si multilayer structures reflecting the light by interlayer interference. Unfortunately, any of these mirrors absorbs about 30% of the incident highly energetic light, which inevitably induc-

es chemical and structural transformations within the optically active zone, affecting the optics lifetime.

Current EUV systems contain at least two condenser multilayer mirrors, six projection multilayer mirrors and a multilayer mask, in sum absorbing overall about 96% (!!!) of the transmitted EUV light. So, the ideal EUV source will need to be much brighter than it is formally needed for the resist exposure. Additionally, the first mirror responsible for collecting the light from plasma space is directly exposed to the plasma and therefore is mostly affected by the high-energy ions and plasma debris.

Another problematic aspect of EUV tools is the off-axis mask illumination. The resulting asymmetry in the diffraction pattern causes shadowing effects that deteriorate pattern adequacy. Also, the EUV short wavelength light increases flare, affecting image quality and increasing Line Edge Roughness/Line Width Roughness (LER/LWR) [19].

Lithography mask is normally protected, using pellicles (thin film dust cover to protect a photomask), from being contaminated with particles. Particle contamination is a critically damaging factor if pellicles will not withstand the harsh 13,5 nm irradiation at the working conditions [15]. Without long-lasting pellicles, mask particle contamination would drastically impact the mask surface adequacy and consecutively the yield. The long-lasting pellicle fabrication is not an issue for the conventional 193 nm lithography. The current lack of any suitable pellicle material capable to withstand EUV irradiation 24/7, is preventing the EUV adoption for HVM.

Heat dissipation. Heating per feature volume is way more intense for EUV photons as compared to DUV photons. In addition, EUV lithography tool is prone to slower heat dissipation due to the vacuum conditions in contrast to the DUV one: most of the EUV LPP-released energy is absorbed by the machine walls and reflecting optics and the mask, and only a very small portion, just few %, reaches the wafer and exposes the resist. Heating is a particularly serious issue for the mirror optics and the mask, especially because the heat is absorbed near the surface, right where the mask reflection action takes place. Thereby, if an intense water cooling is decided to be used, an expected associated mask micro-, actually nanovibration, may become an extremely serious concern.

Heating of the EUV mask pellicle film, temperature of which may get up to about 400-450 °C, is also a critical concern, due to the film thermal degradation, deformation and transmission deterioration [15].

It also was recently found that contamination of the multilayer optics is highly influenced by the photoelectron generation and secondary electron yield.

Since EUV light energy is highly absorbed by any material, the EUV irradiated optical components are susceptible to photo-ablation damage (pitting). A number of researchers reported that a Mo/Si multilayer starts showing damage already due to a single pulse of energy as low as 30 mJ/cm^2, and the damage threshold is getting lower with sequential pulses due to cumulative effects.

Optics, mask and wafer defectivity inspection tools. Significant reduction in the number and size of mirror and mask (including the blanks) for defects is critical due to their directly linked yield and reliability losses. Continuous progress in defectivity reduction is gradually taking place, but improvements in reticle fabrication and quality control infrastructure are lagging behind, requiring close focus on related improvements in optics quality (lenses, masks, starting with blanks), as well as techniques to monitor and mitigate the associated defectivity.

For mask and wafer inspection, without which the EUV lithography cannot be considered feasible in the HVM environment, development of a suitable EUV source is in focus as well. It also requires an EUV source, with less power but with higher brightness and better pulse-to-pulse energy and spatial stability. It was shown that a slightly modified plasma source could be also suitable to work for the inspection tool. However, in order to meet the energy and spatial stability specifications, it will require a higher stability plasma vapor generator to be developed. Several advanced approaches are currently under intense development with two of them being the most promising ones: (1) a conventional droplet generator using molten tin alloy droplets as a fuel; (2) a new “no debris” approach, based on the usage of liquid lithium vapor jet as a target, having a self-cleaning input and output windows [20]. The new concept provides a number of advantages, providing higher EUV dose stability and longer optics lifetime, which makes this concept to be highly attractive.

Significant progress toward HVM readiness has been made in EUV mask fabrication and its quality control that enabled the demonstration of EUV production feasibility and good wafer yield, printed with defect free masks. However, to be fully ready for high-volume manufacturing, some major improvements are still needed in mask materials, fabrication processes, defect inspection and distribution metrology and mask protection with a pellicle during use. In particular, pellicle and mask inspection are the two most critical areas of development in the overall EUV mask infrastructure.

Resist. The transition from laboratory to pilot line is absolutely necessary for learning about the actual fabrication issues in order to bring EUV to HVM. Substantial improvements in EUV source power and its reliability are still necessary for EUV lithography to become cost effective as compared to IL MP DUV. However, it sounds doable at the source current state-of-the-art and accumulated knowledgebase. Applicability of the EUV to pitches below 30 nm currently appears to be limited by resist capability, so significant improvement in resist materials is needed to ensure the EUV suitability for the advanced future nodes. CARs may not be capable to do the job due to too small, and thereby, statistically unstable number of the large AG molecules capable to nest within the ENSE element (the so-called resist AG shot noise). The AG Poissonian shot noise problem directly affecting the critical LER parameter, given the large size of the AG molecules, sounds to be another (this time resist associated) fundamental problem, way harsher than the already discussed above Poissonian fluctuations of the number of atoms within the ENSE element.

The interaction of the EUV radiation with the photoresist is absolutely critical, and these fundamentals still remain poorly understood. The 92 eV EUV photons and generated electrons may move via additional pathways different than those by the current 6.4 eV DUV photons. EUV photons will excite and ionize both valence and core electrons, with a high probability of inducing undesirable selective fragmentation of resist molecules containing heavy atoms. Design and optimization of EUV suitable photoresists appears to be impossible without fundamental understanding of the complex EUV induced resist chemistry. Resists, incorporating high absorption cross-section elements, efficiently absorb EUV photons by core electrons, releasing primary and secondary (Auger) low-energy electrons (~80 eV), which are highly efficient in catalyzing uncontrollable chemical transformations during the resists EUV exposure. The mechanisms via which these electrons interact with resist components are the key factors to get the required performance of EUV resists and EUV lithography as a whole.

The EUV source intensity and the resist sensitivity are complementary parameters. It is necessary to increase the EUV resist sensitivity to compensate for the low intensity of the light source and also to reduce the cost of the development and the maintenance of high power EUV exposure systems. However, improving the resist sensitivity is challenging due to the following:

- Getting a comprehensive balance in resolution, LER, and sensitivity (so-called RLS trade-off), is linked to the AG density (number per ENSE), requiring a new resist concept.

- Understanding the resist transformation mechanisms and the reasons of the potential differences between the conventional KrF / ArF photoresists photochemistry in and EUV/EB resists radiation chemistry, especially as far as the AG mechanisms is concerned.

- Improved models of radiation-induced chemistry and a resist pattern formation for EUV CARs based on a number of experimental and simulation works were recently carried out, hopefully, to yield some family of EUV suitable resists.

To summarize this section. Unfortunately, given the recurring delays in the HIV readiness, the value of EUV single exposure has been progressively falling with each missed milestone and requirements for an increased source power beyond 250 W. Considering future patterning and productivity requirements at the 5 nm technology node and beyond, sources powers of 500-1000 W at a reduced operational cost per wafer may seemingly be demanded making the implementation of the EUV lithography for HVM very problematic.

Due to the above discussed obstacles and complications the EUV still stays far from the HVM. The leading edge industry and academic forerunners, not waiting for the lagging EUV equipment providers, are searching and finding solutions utilizing the options available on the plate in real time. Quite a number of successful uses of MP IL DUV were demonstrated in cases where EUV had been previously planned to be used.

As far as the investments is concerned, the industry has spent stunning $15-20 billion on EUV over the years. Despite this really un-comparable investment, the EUV still does not look as commercially viable. Strangely, nevertheless, that the EUV is still considered as the primary technology for the future advanced nodes and the advanced DUV just as its back up.

SC MANUFACTURING EQUIPMENT AND PROCESS CONTROL METROLOGY (SC ME&PCM) BUSINESS ASSOCIATED COMPLICATIONS

SC ME&PCM and Production FAB costs.

A typical FAB production line will have several hundred ME&PCM units. Fabrication devices, being outstandingly accurate and equipped with the necessary quality control tools, are extremely expensive: the common units are priced up to $5 million each, with some of them, like the modern lithography steppers, over $50 million, and as far as the EUV tool cost is concerned, it is even scary to guess.

The SC industry is extremely capital-intensive, with progressively increasing YoY ME&PCM costs. At some point it may start to be constrained with the maximum amount of capital that can be mobilized and invested by a single company, or a consortium, in construction of new R&D and fabrication facilities. Rock's law (RL, named for Arthur Rock [21], an early investor in major firms including Intel, Apple Computer, Scientific Data Systems and Teledyne) also known as Moor's second law (ML2), states that the cost of a SC chip fabrication plant doubles every four years [22]. As of 2015, the associated price had already reached about $14 billion. RL can be seen as economically "other side of the coin" as related to ML (ML1 from now on). At some point, ML2 may start interfering with ML1.

Obsolescence [23]. At this point I would like to refer the reader to a trend termed "obsolescence", which, in a way, should be considered as being in an opposing connotation to ML. Obsolescence [23] is the state of matters, "which occurs when an object, service, or practice is no longer wanted even though it may still be in good working order. Obsolescence frequently occurs because a replacement has become available that has, in sum, more advantages compared to the disadvantages incurred by maintaining or repairing the original facility"

As technologies rapidly progress, the innovation improvements may become disruptive to cause predecessor technologies to be obsoleted partially and, frequently, completely. However, in situations in which security and survivability of the hardware or data to be obsoleted are paramount, rapid obsolescence may pose obstacles to its straightforward implementation [24]. Also, because toxic materials are used in the production of modern chips, the obsolescence, if not properly handled, may lead to harmful environmental impacts.

On the economic side, the obsolescence may sometimes be helping companies to profit greatly from the regular purchase of new equipment instead of retaining an old device for a longer period of time.

The more advanced technology is used by a new FAB, the higher is the probability that the old FAB will be obsoleted once the advanced production starts. Intel, for example, was known to build new FABs to run the advanced technology nodes. Except, probably, the recent case. On February 18, 2011, Intel announced that it would start constructing a new $5 billion SC facility (FAB 42), "the most advanced, high-volume manufacturing facility in the world," in Arizona, to come on line in 2013 manufacturing 14 nm chips [25]. Later Intel has decided to postpone opening this facility and instead upgrade its existing facilities to support 14-nm chips [25]. This is just an example that even for companies as advanced and economically powerful as Intel, the FAB obsolescence may not always be the best business decision. Especially because the extremely high cost of constructing a new advanced FAB may not meet the related estimations of the Return of Investment. Especially lately for Intel, when the market's attention is focused on mobile products and less on PCs.

Typically, as it was mentioned above, the leading chip-fabrication companies build completely new FABs for advanced nodes, which creates an added problem, namely, what to do with the old FABs. Some companies adjust older FABs for making less advanced products, other companies rent it out and some close it entirely, because the upgrading cost may exceed the cost of a new FAB.

Wafer size [26] and FAB automation trends. There is a lasting trend to use in production ever larger wafers, allowing to process more chips at once printed on the same wafer, helping to minimize production costs per chip. Currently, the forth runners use in the production and pilot lines 300 mm (12 inch) wafers, but the industry is already considering a probability of transferring to 450 mm (17,7 inch) wafer size some time by 2018-2020.

Besides, there is a drive for full automation of the production lines, which is often referred to as the "lights-out FAB" concept [27], which will certainly require a lot of attention to the real time PCS.

Globalization [28]. Growth in consumer and industrial electronics global demand (smartphones, tablets, digital televisions, wireless communication infrastructure, network hardware, computers and electro-medical devices) continues its push for even more advanced SC chips enriched with advanced functionalities. Globalization, in general, has a number of *pros*, but also some *cons*, knowledge on which is very helpful to prevent and/or cope after undesirable developments in the business environment.

The US SC industry is the leading provider of the SCs to the world. The US SC ME&PCM sector accounts for roughly 50% share of the world market. However, over 80% of US SC sales and 84% of SC ME&PCM sales take place overseas, so, US companies MUST export. Top markets for US SCs and SC ME&PCM are China, the EU, Japan, Korea (South), Singapore and Taiwan.

The newly developing SC business sector, Internet of Things (IoT) – otherwise, variety of Internet Connected Devices – is in its early growth stage, but already contributes significantly to SC demand in

long-term, as well as the growth of smart grids, smart cities and automated smart manufacturing.

In the SC ME&PCM space, the business is as usual (SC fabrication devices), expected worldwide 13,2% growth from 2016 to 2017 (to an estimated $42,8 billion) driven by equipment for foundries, and for memory and power chip fabrication. For the wafer FAB equipment shipments are expected to grow 2,5% YoY starting 2016, however, some pessimistic business analysts paint a downsize picture for the ME&PCM market, with a 2,5% fall in 2016 prior returning to the growth in 2017.

SC ME&PCM providers (AMAT, TEL, Lam Research, KLA-Tencor, ATML and others) expect fabrication companies to increase 14 nm and 16 nm capacity and start investing in 10 nm production in 2016. Samsung expects both 16 nm/14 nm, and 10 nm technologies to run in parallel for quite some long time. China plans to start or complete eight new FABs in 2015-2016, outstripping planned facilities in Taiwan and Southeast Asia, with 5 new FABs each, the US with 4; and Korea (South), Europe and the Middle East, with 1 each. All of these 25(!!!) new facilities, should construction go on, will need to be equipped in the 2016 to 2018 time-period.

R&D costs for SC as well as for SC ME&PCM technologies are growing significantly for each advanced node, creating tough business conditions and pushing both fabrication and ME&PCM companies to consider consolidation and/or join their efforts in running the R&D. The uncertain economic environment makes it difficult to predict (guaranteed) the SC ME&PCM business growth due its derivative dependence from the SC fabrication business, resulting in consolidation, which already has started in the ME&PCM market: in October 2015, Lam Research Corp. agreed to acquire KLA-Tencor for $10.6 billion [29].

Notably, historical trends show that the major SC production companies, not willing to accept the risk dealing with small financially not stable entities, stimulate small companies to give up their business, frequently very technically promising, to the “big brothers”, also promoting consolidation.

A couple of marketplace trends:

New Business Entry – The cost of SC business entry is extremely painful or even impossible for all but the biggest players capable to keep up with state-of-the-art operations. It comes as no surprise that established players have a big advantage and even appearance and success of "fabless" chip makers is just an evidence of the power of the big well established entities.

Bargaining power – For the large SC companies, suppliers have little bargaining power – big SC companies have hundreds of suppliers. This diffusion of risk over many companies allows the chip giants to keep the bargaining power of any single supplier to a minimum. As to the SC ME&PCM suppliers of cutting-edge equipment and process, while consolidating, these companies at their turn gain some increased bargaining power. The buyers have little bargaining power dealing with a small number giant SC chip makers.

Threat of Substitutes – The intellectual property protection might stop the threat of advanced substitute chips for some time. However, within a short period of time copy-cat companies start to produce similar advanced products at lower prices. A SC company spends millions, if not billions, on creation an advanced chip, but at some point comes a player that runs the chip reverse engineering and makes and markets a similar product for a fraction of price.

Competitive Rivalry. The industry is marked by intense competition between companies. There is always pressure on chip makers to come up with something better, faster and cheaper than the latest state-of-the-art, which extends to everyone involved in the business of providing the chips to the marketplace.

Cyclic nature of the SC and SC ME&PCM business [30]. I cannot resist but to start this paragraph with the following citation, which I like very much: “*If SC investors can remember one thing, it should be that the SC industry is highly cyclical.”* SC sales historically were closely following the world’s GDP growth at various reasonably reproducible cycle times experiencing upturns and downturns. The cyclical nature of the SC industry and periodic overcapacity make this industry particularly vulnerable to significant and sometimes prolonged economic downturns.

Consumer trends directly influence the SC industry. For instance, consumers shift from PC to mobile had a painful impact on Intel’s revenue, as Intel was heavily dependent on PC sales. On a positive note on Intel, when the world shifted to cloud computing Intel swiftly adopted this concept and gained a share greater than 95% of the data center market.

The seasonal sales trends for SC services and products closely follow trends for consumer electronics, communication, and computer sales. These SC sales, in their turn, influence the ME&PCM sales and new equipment orders. It looks like the associated periodicity could be modelled and used to predict the upturns and downturns and build-up preventive measures. Unfortunately, the history shows, that the predictability of such models is not highly reliable,

especially, when strong (political or economic) market shake-ups take place. So, companies are not willing to accept such a risk and assurance that the actual market variations will meet the model-based expectations, because any not anticipated change in the assumed seasonal variations may result in adverse, or even catastrophic effects on company revenues, operations and overall businesses. "The trend is your friend, until the opposite"- as stock market traders say.

Summarizing:

- SC ME&PCM business, following the state of the chip fabrication companies, is strongly cyclic.

- The forecasts for the next couple of years indicates observable growth.

- The US SC industry is the leading provider of the SCs to the world, US companies also lead in the SC ME&PCM.

- Intense globalization is spreading over the SC fabrication as well as over the SC ME&PCM sectors, strongly influencing the SC business environment, imposing its *pros*, and *cons* and triggering consolidations even among the leading SC ME&PCM companies.

Advanced process support, process monitoring metrology concepts and HW. Just to mention quickly a field that naturally is on the SC equipment leading edge and heavy demand – it is the wafer and mask quality inspection and assessment. Specifically, the so-called *in situ* real-time inspection tools, watching the processed wafer or mask while they are in process, and capable to detect and communicate about a problem and trigger the necessary corrective actions immediately once the problem happened, are on a keen demand, specifically thanks to the "lights-out FAB" full automation trend.

Taiwan has consistently been the top global SC ME&PCM market in recent years, representing over a quarter of the total worldwide market with the US as the top importer of SC ME&PCM into Taiwan. Taiwanese foundries TSMC and UMC are both global leaders in SC manufacturing and buy state-of-the-art SC ME&PCM. TSMC is ranked second globally in estimated capital spending, UMC is ranked eighth. There are also a number of smaller SC manufacturers in Taiwan, primarily in the memory segment, that also purchase SC ME&PCM.

Challenges and Barriers to US SC and related equipment exports. There are no significant barriers to US SC or SC ME&PCM exports to Taiwan. As a participant in the WTO Information Technology Agreement (WTO ITA) and its recent expansion, Taiwan allows imports of most SCs and related ME&PCM to enter duty-free. Taiwan is open to deals in both SCs and SC ME&PCM and presents a good market for US companies. Many US fabless SC companies directly benefit from contracting production of their IC designs to Taiwan.

SC BUSINESS ENVIRONMENT. THE COST FACTOR: EXTREMELY HIGH R&D AND PRODUCTION FAB COSTS

Production FAB costs. The SC industry is extremely capital-intensive, with progressively increasing YoY ME&PCM costs. At some point the integrated costs may start to be constrained due to the maximum amount of capital that can be mobilized and invested in advanced production or R&D by a single company, or a consortium. Statistics shows the cost of putting together a new FAB starts at over $1 billion with values as high as $3-4 billion being pretty common. As an extreme example, TSMC invested $ 9.3 billion in its mammoth FAB15 fabrication facility [31].

Normally, once the chip-fabrication companies built a completely new FABs for advanced node, it creates a new associated problem, namely, what to do with the obsoleted ones. Some companies adjust older FABs process to make less advanced products, other companies rent the FAB out and some close it entirely, because the poorly controllable upgrading cost may exceed the cost of building a new FAB. So, yes, "dead" FABs symptomize a specific new SC industry problem.

Enormous R&D and R&D facilities costs. R&D is a critical fueling sector of the SC industry enabling many key breakthroughs in both the production and business spaces. The SC companies worldwide spent in 2015 a total of $56.4 billion in R&D alone, which makes about 17% of the sales, with Intel's alone contribution of 22% of it. The advanced technology R&D costs, as well as, the costs of the SC ME&PCM technologies are growing significantly for each advanced node (remember the ML2), pushing both fabrication and SC ME&PCM companies to consider consolidation and/or joining the efforts in running the R&D. As the costs soar, the industry tends to collaborate more than ever before. "We are doing three nodes at the same time in our R&D center. How can we make it happen? We need tools, materials and open innovation. Also, we cannot do it all by ourselves." – shared his concerns E.S. Jung, executive VP of the SC R&D center at Samsung [32]. As it was mentioned in the previous section, to cope with the economic stress the SC industry already goes through a round of mergers and acquisitions, and it looks like this trend may even accelerate in the nearby future.

The SC ME&PCM market is expected to grow 3.7 % in 2016, followed by 13% in 2017. Taiwan is expected to be a large contributor to the growth in 2017, with five semiconductor FABs starting construction in 2015 to 2016, which are planned to be equipped starting 2017. Taiwan, who overtook South Korea in 2015 to become the world leader in IC FAB capacity, is forecasted to remain the top market for semiconductor SC ME.

Samsung, TSMC and Intel are forecasted to spend a combined 45% of the total semiconductor industry outlays in 2016 [33]: Samsung's full-year 2016 capex budget is US$11.0 billion, TSMC's – US$10.0 billion and Intel's – US$9.5 billion

Just recently TSMC announced it already had purchased equipment from U.S. semiconductor ME&PCM companies Applied Materials and Lam Research and KLA for a total of about $8.6 billion, and ASE (Taiwan), the top-ranked OSAT (outsourced assembly and test) company in the world, announced three purchases of semiconductor assembly and test equipment for a total of about $52.6 million from Kulicke&Soffa (US), Besi (Netherlands) and Disco Corporation (Japan) [34].

Globalization *pros* and *cons*. Globalization is a tendency of open systems in general, and industrial and business systems in particular, to undergo in a free space an unlimited unimpeded expansion, which can be slowed down and even completely stopped while running into a barred environment) confined with barriers due to political or religious or otherwise considerations) naturally creating economically isolated islands. Globalization achieves its greatest power when it is truly global free; when it provides the means to access to the information systems and research centers in other countries and establish arrangements that promote the cooperation and transfer of technology.

The essence of the modern economic globalization is associated with a greater role of the multinational enterprises and foreign direct investment that increasingly integrates the world economy. Multinational enterprises engage in worldwide investments: (a) to gain access to overseas markets and (b) to gain access to less expensive labor or to raw materials or energy. In the same time, it helps developing economies to grow and mature and effectively compete in world markets, which makes this engagement, in its essence, bi-directional (G&G) – Get and Give.

Globalization is an extensively broad and multi-faceted theme [35] extending far out of the frame of these quick notes, so I am trying to keep it directly to the SC point, as it was defined in the paper's purpose statement. Remembering the defined goal to deal primarily with the SC industry challenges, I, nevertheless, would like to refer the reader to one of the greatest positive aspects of globalization, namely, to the effect of balancing the world tensions by the multi-national enterprises [36]. Indeed, governments play a central role at the national level. However, the politicians, realizing the impact of technology on world events, today consider the industry related questions almost at each and every political discussion. National interests differ from nation to nation due to specifics of regulations, procurement, protectionist policies, and capabilities to support the global R&D. Public opinions also differ and these differences influence the governmental policy. Each country follows its own way of dealing with globalization. As a result, countries move forward at different rates, sometimes even in different directions causing international imbalances and stress. In this sense, multinational corporations and transnational joint ventures serve as buffers promoting vital global balance.

Relevantly to the SC business [37], the globalization helps getting access to less expansive highly educated resources and to wider consumer market, which assists both in mitigating the costs and in improving the effectiveness of the R&D investments.

The geography of the current competitive "globalized" SC world could be depicted as follows:

The US – is the main hub for the R&D activities in the SC industry; five of the top ten SC companies in the world are US-based. At the end of 2015, the US government passed legislation expanding the R&D tax credit permanently, thus stimulating R&D spending by companies and crediting the start-ups.

Taiwan – with its well established set of advanced foundries and R&D entities, as well as the proven infrastructure of the production supporting businesses, Taiwan is considered to be one of the leading centers of the SC industry.

China - to become self-sufficient in the SC fabrication infrastructure China considers acquiring several relevant companies in the US and Taiwan and also invites SC companies to build FABs in the mainland. Intel and TSMC already announced plans to build and/or upgrade fabrication facilities in China. Unfortunately, China's weak IP protection has long been a cause of long lasting tension with the US, which affects the SC business between the two.

Japan has the world's largest 200mm wafer fabrication capacity, which makes it a great production base for various SC chips. Unfortunately, Japanese SC business leaders missed the latest smartphone trend, which led to bankruptcies of several Japanese SC companies.

European Union – the conditions here are very complicated due to Europe multifaceted economic and political crises. Germany, with its strong demand by automotive and industrial electronics, is driving SC growth in Europe. Western Europe has the cultural tradition and core of excellent research groups to facilitate its leading position in the technology arena. Yet, additionally to existing crises, it lacks the cohesion, which is absolutely necessary to develop strategic world initiatives in important sectors.

Eastern Europe and Russia – well, not too much yet…

Rapid changes and especially the high tech industry expansion can proceed freely globally only when the globalization supporting systems provide a real time, or at least quick, access to the communication and information systems between the countries. It is an absolutely MUST condition, because it allows to establish timely arrangements, promoting easy and fast technology and innovation exchange, to avoid or quickly to correct conflicting situations. Communication and technology exchange resources, timely established agreements and regulations are vital for global technology expansion, which requires absence of economic conflicts, surprises and wrongdoings. Unfortunately, in spite of availability of superfast modern communications, this effort is sometimes constrained due to bureaucratic inertia, protectionism, concerns about intellectual property, existing alliances, national security. Also, in some cases national phobias and conspiracy false speculations create barriers impeding nations to achieve economic growth necessary to close the gap with leading nations and harness from globalization.

The old temptation of the developed companies to go overseas just to gain access to inexpensive labor was working distinctly well in the past mainly in low tech industries. But with the rise of China and India and other East Asia countries, the US leadership in sophisticated technological production and the associated benefits in terms of jobs and wealth creation, became no longer to be given as granted. Globalization causes inevitable diffusion of experience and knowledge, and together with these matters also dissipate the wealth growth rate and employment. With relevance to the US economy the advantage that in the past was acquired via US advanced industries is little by little diffusing nowadays. Having Intel and Micron, fabless Qualcomm, leading SC ME&PCMs (AMAT, Lam Research (&KLA) and others) on its soil, the US is not losing the leading edge and it does not look like it will lose it anytime soon. US is still a key center for knowledge creation and its dissemination, even though it is in increasingly tough competition with other world locations specializing in high tech industries [38].

CONCLUSIVE REMARKS

Referring to the purpose definition of these notes – share with readers my views on some current hot matters in the SC industry – I would like to highlight that the term "current" is very illusive while considering the state of the art of this industry. The SC technology is progressing so swiftly that whatever looks as a fresh update, in this extremely competitive industrial Multiverse [39] may become an old story by the time the report is finalized.

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